CBCS SCHEME

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15EC61

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define Hilbert transform. What are its applications. Prove that a signal g(t) and its Hilbert transform $\tilde{g}(t)$ are orthogonal over the entire time interval $(-\infty, \infty)$. **(05 Marks)**

b. Determine the pre-envelope and complex envelope of the RF pulse defined by $x(t) = A\,\text{rect}\left(\frac{t}{T}\right)\cos(2\pi f_c t)$. **(06 Marks)**

c. Compare the power spectra of various line codes in terms of bandwidth, DC component, Noise immunity and synchronization capability, with neat sketch. **(05 Marks)**

OR

2 a. Express bandpass signal s(t) in canonical form. Also explain the scheme for deriving the inphase and quadrature components of the bandpass signal s(t). **(06 Marks)**

b. Explain with relevant expressions, the procedure for computational analysis of a bandpass system driven by a bandpass signal. **(06 Marks)**

c. What is the advantage of HDB3 code over conventional alternate mark inversion(AMI) code. Code the pattern "1010000011000011000000" using HDB3 encoding and AMI encoding. **(04 Marks)**

Module-2

3 a. Explain the geometric representation of set of M energy signals as linear combination of N orthonormal basis functions. illustrate for the case N = 2 and M = 3, with necessary diagrams and expressions. **(08 Marks)**

b. Using the Gram–Schmidt orthogonalization procedure, find a set of orthonormal basic functions to represent the three signals $s_1(t)$, $s_2(t)$ and $s_3(t)$ shown in Fig.Q3(b). also express each of these signals in terms of the set of basis functions. **(08 Marks)**

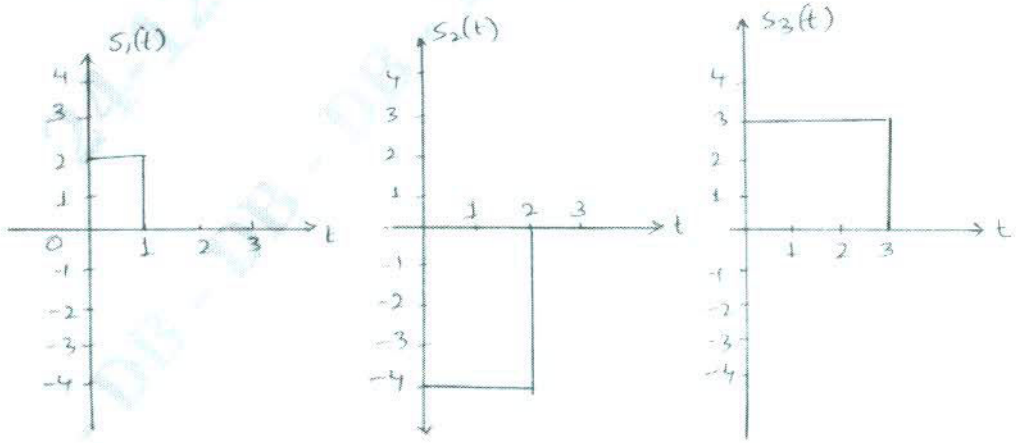

Fig.Q3(b)

OR

4 a. Explain the correlation receiver with neat diagrams and explanation of detector and the maximum –linklihood decoder blocks. **(08 Marks)**

b. Explain the matched filter receiver. Obtain the expression for the impulse response of the matched filter. **(08 Marks)**

Module-3

5 a. Derive the expression for error probability of binary PSK using coherent detection. **(06 Marks)**

b. Binary data are transmitted over a microwave link at the rate of 10^6 bits/sec and the power spectral density of the noise at the receiver input is 10^{-10} ω/Hz. find the average carrier power required to maintain an average probability of error $Pe \leq 10^{-4}$ for the following cases.
Binary PSK using coherent detection
DPSK
Note : take $erfc(2.63) = 2 \times 10^{-4}$, $Q(3.7) = 10^{-4}$. **(06 Marks)**

c. Define bandwidth efficiency. Tabulate and comment on the bandwidth efficiency of M-ary PSK signals for different values of M. **(04 Marks)**

OR

6 a. With neat diagram and expressions, explain binary FSK generation and non-coherent detection scheme. **(06 Marks)**

b. Explain the generation and optimum detection of differential phase – shift keying with neat block diagram. **(06 Marks)**

c. What is the advantage of M-ary QAM over M-ary PSK system? Obtain the constellation of QAM for M = 4 and draw signal space diagram. **(04 Marks)**

Module-4

7 a. With a neat block diagram, explain the digital PAM transmission through band limited baseband channels. Also obtain the expression for inter symbol interference. **(06 Marks)**

b. Explain the modified duo-binary signaling scheme, with pre-coding. Illustrate the encoding for the binary sequence "011100101". Assume previous pre-coder outputs as 1. **(07 Marks)**
With neat diagram, explain the timing features pertaining to eye diagram and it interpretation for baseband binary data transmission system. **(03 Marks)**

OR

8 a. With neat sketches and expressions, explain raised cosine spectrum solution to reduce ISI. **(06 Marks)**

b. What is the advantage of controlled ISI partial response signaling scheme? With block diagram, explain the duo-binary encoder with pre-coder. Mention the frequency response, impulse response and its features. **(06 Marks)**

c. With neat diagram and relevant expressions, explain the concept of adaptive equalization. **(04 Marks)**

Module-5

9 a. Explain the working of Direct Sequence Spread Spectrum transmitter and receiver with neat diagram, waveform and expressions. **(08 Marks)**

b. A slow frequency Hopped/MFSK system has the following parameters,
   i) The number of bits/MFSK symbol = 4
   ii) The number of MFSK symbols per hop = 5
   iii) Calculate the processing gain of the system in decibels. **(03 Marks)**

c. List and briefly explain any 3 applications of direct sequence spread spectrum. **(05 Marks)**

OR

10 a. With a neat block diagram, explain frequency Hopped spread spectrum technique. Explain the terms chip rate, Jamming Margin and processing gain. **(08 Marks)**

b. What is a PN sequence? Explain the generation of maximum-length sequences (ML-sequence). What are the properties of ML sequences? **(04 Marks)**

c. In a DS/BPSK system, the feedback shift register used to generate the PN sequence has length m = 19. The system is required to have an average probability of symbol error due to externally generated interfering signals that does not exceed 10^{-5}. Calculate the following system parameters in decibels :
   i) Processing gain
   ii) Antijam margin
   (Assume Q(4.25) = 10 –5 or erfc(3) = 2×10^{-5}). **(04 Marks)**

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15EC62

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
ARM Microcontroller and Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain architectural features of cortex M3 with block diagram. **(07 Marks)**
b. Briefly describe the special registers of cortex M3. **(06 Marks)**
c. What is stack and what are the instructions to access stack? **(03 Marks)**

OR

2 a. Briefly discuss features of built in nested vector interrupt controller. **(08 Marks)**
b. Write a short note on :
i) Debugging support
ii) Interrupts and exceptions supported by cortex M3. **(08 Marks)**

Module-2

3 a. Explain memory map of cortex M3 with diagram. **(08 Marks)**
b. Write C language program to toggle an LED with small delay in cortex M3. **(05 Marks)**
c. Explain the 32 bit multiply instruction set. **(03 Marks)**

OR

4 a. Explain arithmetic instruction set with example. **(07 Marks)**
b. Briefly explain shift and rotate instructions with diagrams. **(07 Marks)**
c. Explain working of following instructions :
i) CMP ii) TST iii) CMN iv) REV. **(02 Marks)**

Module-3

5 a. Explain the sequence of operations for communicating with an I2C slave device. **(08 Marks)**
b. Write the differences between :
i) RISC and CISC
ii) Harvard architecture and Von Neumann architecture. **(08 Marks)**

OR

6 a. Briefly explain PLDs and types of PLDs. **(06 Marks)**
b. Write short note on :
i) Optocoupler
ii) COTS. **(08 Marks)**
c. Explain working of DRAM. **(02 Marks)**

Module-4

7 a. List and explain characteristics of an embedded system. **(06 Marks)**

b. Briefly describe any two operational and two non operational quality attributes. **(08 Marks)**

c. Define and classify electronic control units. **(02 Marks)**

OR

8 a. Discuss fundamental issues in hardware software co-design. **(08 Marks)**

b. Differentiate between DFG and CDFG with example. **(04 Marks)**

c. Explain different types of serial interface buses deployed in automatic embedded application. **(04 Marks)**

Module-5

9 a. Define process and explain process states and states transition diagram. **(07 Marks)**

b. Explain functional requirements to be analysed in selection of an RTOS. **(06 Marks)**

c. Differentiate between threads and process. **(03 Marks)**

OR

10 a. Explain round robin scheduling technique. **(03 Marks)**

b. Three process with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 ms respectively enters ready queue together. A new process P4 with estimated completion time 2ms enters ready queue after 2ms. Calculate waiting time, turnaround time and average turnaround time with help of preemptive SJF scheduling. **(10 Marks)**

c. Explain concept of pipe for IPC. **(03 Marks)**

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15EC63

Sixth Semester B.E. Degree Examination, Dec.2018/Jan. 2019
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Mention any two differences between CMOS and Bipolar technology. **(02 Marks)**

b. Write all the mask steps of p-well process. **(06 Marks)**

c. With neat diagrams, explain the cut off, linear and saturation regions formation in MOSFET with different values of V_{gs} and V_{ds}. **(08 Marks)**

OR

2 a. Explain body effect as non ideal IV effects of MOSFET. **(03 Marks)**

b. Explain Noise margin, with respect to CMOS inverter. **(05 Marks)**

c. Explain the steps of n-MOS fabrication with neat diagram. **(08 Marks)**

Module-2

3 a. With a neat diagram, explain λ - rules for buried and butting contact and show thE cross sectional view of same. (white any one structure burreid contact). **(08 Marks)**

b. Estimate the rise time and fall time of a CMOS inverter and summarise the result. **(08 Marks)**

OR

4 a. Define sheet resistance, with equation. **(02 Marks)**

b. Calculate the area capacitance of the layer below [Refer Fig.Q4(b)] :

Fig.Q4(b)

i) If the layer is metal – 1 and relative capacitance value is 0.075 C_g

ii) if the layer is polysilicon and relative capacitance value is 0.1 C_g. **(06 Marks)**

c. Write the schematic and stick diagram for Boolean expression $y = \overline{(a + bc)}$.(implement using CMOS logic). **(08 Marks)**

Module-3

5 a. Design a 4bit, 4 × 4 barrel shifter. Write the nMOS implementation and strategy for the same. **(08 Marks)**

b. Explain carry select adder with neat block diagram. **(08 Marks)**

OR

6 a. Define regularity. **(02 Marks)**

b. Derive the scaling factor for the device parameter :
   i) Parasitic capacitance
   ii) Channel resistance
   iii) Gate delay. **(06 Marks)**

c. Implement the ALU functions like EX-OR, EX-NOR AND and OR operations with an adder. Write the block diagram of 4-bit ALU using adder element. **(08 Marks)**

Module-4

7 a. Explain the following logics :
   i) Clocked CMOS logic
   ii) n-p CMOS logic. **(08 Marks)**

b. Explain parity generator, with the nMOS implementation of parity generator with stick diagram. **(08 Marks)**

OR

8 a. Explain Pseudo-nMOS logic. Find Z_{pu}/Z_{pd} when $V_{inr} = 0.5V_{DD}$, $V_{tn} = |V_{t_p}| = 0.2V_{DD}$, $V_{DD} = 5V$ and $\mu_n = 2.5\mu p$. **(08 Marks)**

b. Explain the 4-way data selector (multiplexer) with Boolean equation and nMOS based stick diagram. **(08 Marks)**

Module-5

9 a. Write the system timing considerations. **(08 Marks)**

b. Explain logic verification principle. **(08 Marks)**

OR

10 a. Explain three transistor dynamic RAM with neat circuit and stick diagram. **(06 Marks)**

b. What are design manufacturability. **(10 Marks)**

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15TE63

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Microwave Theory and Antennas

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Discuss the mechanism of oscillation and also mode oscillation reflux Klystron oscillator. **(08 Marks)**

b. Derive the transmission line equations and also solution for the same. **(08 Marks)**

OR

2 a. Derive the expressions for reflection coefficient and transmission coefficients. **(08 Marks)**

b. A 50Ω coaxial line operating with wavelength 1 metre is terminated with an impedance of 60-j80Ω. Design a single stub matching system to avoid standing waves using smith chart. **(08 Marks)**

Module-2

3 a. Show how the S-matrix is derived for a multiport network. **(08 Marks)**

b. Discuss the properties of S-parameters in detail. **(08 Marks)**

OR

4 a. With a neat diagram explain the operating principle of two hole directional coupler and also derive its S-matrix. **(08 Marks)**

b. With a neat diagram, explain faraday rotation isolator. **(08 Marks)**

Module-3

5 a. Discuss the different losses occurred in microstrip line. **(08 Marks)**

b. A loss less parallel stripline has a conducting strip width W. The relative dielectric constant ε_{rd} of the substrate is 6 and a thickness d of 4mm.
Calculate:
i) The width W of the conducting strip in order to have characteristic impedance of 50Ω.
ii) Strip line capacitance
iii) Strip line inductance
iv) The phase velocity of the wave in the parallel strip line. **(08 Marks)**

OR

6 a. Explain the following antenna parameters:
i) Beam solid angle
ii) Radiation intensity
iii) Half power beam width
iv) Directivity. **(08 Marks)**

b. Derive FRII's transmission formula for radio communication link. **(08 Marks)**

Module-4

7 a. Derive the resultant radiation pattern for an array of two isotropic point sources placed $\lambda/2$ distance apart and fed with power of equal magnitude and phase. Draw the pattern. **(08 Marks)**

b. State and explain power theorem as applied to a point source. The radiation pattern of a source is given by $u = u_m \sin^2\theta$. Find its directivity for $0 \le \theta \le \pi$, $0 \le \phi \le 2\pi$. **(08 Marks)**

OR

8 a. Obtain an expression for radiation resistance of a short electric dipole. **(08 Marks)**

b. Give a geometry of a short dipole and explain the terms retarded current, retarded scalar potential and retarded vector potential. **(08 Marks)**

Module-5

9 a. Derive an expression for radiation resistance of a small loop antenna. **(08 Marks)**

b. With the help of neat diagrams explain different types of rectangular antennas. **(08 Marks)**

OR

10 a. Discuss practical design considerations for a monofilar axial-mode helical antenna. Draw relevant diagrams wherever necessary. **(08 Marks)**

b. Discuss constructional features of a yagi-uda antenna. Draw a neat diagram of six element yagi-uda antenna with dimensions at 500 MHz. **(08 Marks)**

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15EC64

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Show the encapsulation and decapsulation representation in the TCP/IP model and explain. **(06 Marks)**

b. Define framing, explain role of bit stuffing in a framing. **(04 Marks)**

c. Mention the different network topology. List out advantages and disadvantages of each topology. **(06 Marks)**

OR

2 a. What are five components involved in data communication? Explain with a suitable diagram. **(05 Marks)**

b. Demonstrate stop and wait protocol by considering acknowledgement, timer and sequence no with the help of flow diagram. **(06 Marks)**

c. Describe link layer addressing with suitable illustration. **(05 Marks)**

Module-2

3 a. A ALOHA network transmits 200 bit frame using a shared channel with a 200 kbps band width. Find the through put of pure and slotted ALOHA if the system produces 500 frame per second. **(06 Marks)**

b. Describe the frame format of IEEE 802.3 Ethernet. What are minimum and maximum length of frame? **(07 Marks)**

c. Identify unicast, multicast and broad cast from the following MAC addresses:
4A : 30 : 10 : 21 : 10 : 1A
47 : 20 : 1B : 2E : 08 : EE
FF : FF : FF : FF : FF : FF. **(03 Marks)**

OR

4 a. A network using CSMA/CD has a band width of 10 Mbps. If the maximum propagation time is 25.6μs. What is the minimum size of the frame? **(05 Marks)**

b. Explain polling technique with suitable illustration. **(06 Marks)**

c. In the standard Ethernet with the transmission rate of 10 Mbps, length of cable is 2500 mt and frame size is 512 bits. The propagation speed of a signal in a cable is 2×10^8 m/s. Find efficiency of standard Ethernet. **(05 Marks)**

Module-3

5 a. Explain the following connecting devices: i) Hub ii) Link layer switch iii) Router. **(06 Marks)**

b. Define two types of Bluetooth networks. **(06 Marks)**

c. Differentiate between data gram network and virtual circuit network. **(04 Marks)**

OR

6 a. Define IEEE 802.11 addressing mechanism for four cases. **(06 Marks)**

b. Give a note on virtual LAN. **(05 Marks)**

c. An organization is granted a block of address with the beginning addresses 14.24.74.0/24. The organization need to have 3 sub blocks of addresses to use in its three subnets: one sub block of 10 addresses, one sub block of 60 addresses, and one sub block of 120 addresses. Design the sub blocks. **(05 Marks)**

Module-4

7 a. Give a brief overview of IPV4 datagram. **(10 Marks)**

b. Find the shortest path from source 'A' to destination 'G' from given graph as shown in the Fig.Q.7(b) using the Dijkstra algorithm. **(06 Marks)**

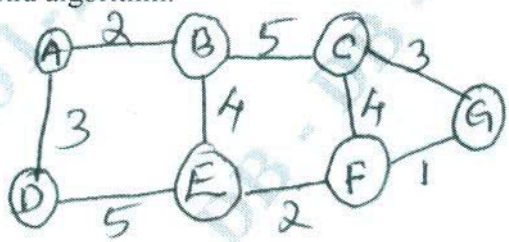

Fig.Q.7(b)

OR

8 a. Explain three phases of communication between a remote host and mobile host. **(08 Marks)**

b. Explain distance-vector-routing using a Bellman Ford algorithm providing a suitable illustration. **(08 Marks)**

Module-5

9 a. Describe connectionless and connection – oriented services provided by the transport layer. **(08 Marks)**

b. Discuss TCP segment. **(08 Marks)**

OR

10 a. Demonstrate Go-back-n protocol with a forward channel is reliable but in the reverse channel, if an acknowledgment is delayed or lost. **(06 Marks)**

b. Explain a TCP connection establishment using three way hand shaking. **(10 Marks)**

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15EC651

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Cellular Mobiles Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. A total of 90MHz of bandwidth is allocated to a FDD cellular telephone system which uses two-30 kHz simplex channels to provide full duplex voice and control channels. Compute the number of channels available per cell if a system uses:
i) 4-cell reuse ii) 7-cell reuse iii) 12-cell reuse. **(06 Marks)**

b. Explain with necessary mathematical equations Okumura model. **(06 Marks)**

c. Explain the following:
i) GOS
ii) Co-channel and adjacent channel interference. **(04 Marks)**

OR

2 a. List the various capacity expansion techniques in cellular system. Explain 60° sectoring and 120° sectoring. **(08 Marks)**

b. Write short notes on log-distance path loss model. **(08 Marks)**

Module-2

3 a. Explain the various factors that influence small scale fading. **(08 Marks)**

b. Explain with necessary mathematical equations Ricean and Rayleigh fading distributions. **(08 Marks)**

OR

4 a. Define the following: i) Coherence time ii) Coherence Bandwidth. **(04 Marks)**

b. Write short notes on frequency selective fading. **(06 Marks)**

c. Consider a transmitter which radiates a sinusoidal carrier frequency of 1850 MHz. For a vehicle moving 60mph, Compute the received carrier frequency if the mobile is moving: i) Directly towards the transmitter ii) Directly away from the transmitter. **(06 Marks)**

Module-3

5 a. With a neat diagram, explain various interfaces in a GSM network. **(08 Marks)**

b. Give the schematic of speech functions at the receiver. **(04 Marks)**

c. Write short notes on IMSI. **(04 Marks)**

OR

6 a. With a neat block diagram, explain briefly the various stages of channel coding. **(06 Marks)**

b. With a neat diagram, explain GSM protocol architecture for signaling. **(10 Marks)**

Module-4

7 a. Explain with a diagram, GSM architecture for HSCSD support. **(06 Marks)**

b. With a neat diagram, explain the location update procedure if there is a change in VLR area. **(10 Marks)**

OR

8 a. List the various services provided in GSM. **(06 Marks)**

b. Explain with a neat diagram GPRS system architecture and interfaces. **(10 Marks)**

Module-5

9 a. With a neat block diagram, explain CDMA architecture. **(10 Marks)**

b. Explain with necessary diagrams, three types of soft CDMA hand off. **(06 Marks)**

OR

10 a. With a neat block diagram, explain the reverse access channel processing of a CDMA system. **(08 Marks)**

b. Explain briefly the various system tasks performed for call setup in CDMA systems. **(08 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain with illustration, a simple design methodology followed in IC industries. **(08 Marks)**

b. Explain the following constraints imposed in real world circuits :
i) Noise margin ii) propagation delay. **(03 Marks)**

c. Develop a verilog model for a 7–segment decoder, include an additional input, blank, that overrides the BCD i/p and causes all segments not to be lit. **(05 Marks)**

OR

2 a. Develop a verilog module of a debouncer for a push button switch that uses a debounce interval of 10ns. Assume the system clock frequency is 50 MHz. **(06 Marks)**

b. Design and develop a circuit and verilog module for modulo 10 counters. **(06 Marks)**

c. What is the distinction between a Moore and Mealy finite state machine? **(04 Marks)**

Module-2

3 a. Write a symbol for basic memory component and explain its parts. **(06 Marks)**

b. Explain about the multiport memories. **(06 Marks)**

c. Compute the 12-bit ECC word corresponding to the 8-bit data word "0110001". **(04 Marks)**

OR

4 a. Design a 64 K × 16 bit composite memory using 16K × 8 bit component. **(08 Marks)**

b. What is the difference between asynchronous static RAM and synchronous static RAM? **(06 Marks)**

c. Using a Hamming code, how many check bits are required for single error correction and double error detection for 4-bit data word? **(02 Marks)**

Module-3

5 a. Design a priority encoder that has 16 inputs, i[0 : 15]; a 4-bit encoded output, z[3 : 0] and a valid output ie. '1' when any input is '1'. Input i[0] has the highest priority and i[15] is the lowest priority. **(08 Marks)**

b. Explain the concept of differential signaling. How does differential signaling improve noise immunity? **(08 Marks)**

OR

6 a. What are the purpose of logic blocks and I/O blocks in FPGA? **(06 Marks)**

b. Explain different types of PCB design. **(03 Marks)**

c. Explain with a neat diagram of the internal organization of a CPLD. **(07 Marks)**

Module-4

7 a. What are the purpose of following in an I/O controller : i) input register ii) output register iii) control register iv) status register. **(06 Marks)**

b. Explain neatly the designing a R-string DAC. **(05 Marks)**

c. Explain about tristate buses and weak drive. **(05 Marks)**

OR

8 a. Design and develop a verilog code for an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut. When input value changes the controller is the only interrupt in the system. **(08 Marks)**

b. What are the serial input standards? Briefly explain each. **(08 Marks)**

Module-5

9 a. Explain the design flow of hardware/software co-design. **(10 Marks)**

b. Briefly describe techniques used in power optimization. **(06 Marks)**

OR

10 a. What is the distinction between logical partition and physical partition? **(08 Marks)**

b. Explain Built-In–Self–Test (BIST) techniques. **(08 Marks)**

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15EC61

Sixth Semester B.E. Degree Examination, July/August 2021
Digital Communication

Time: 3 hrs. Max. Marks:80

Note: ***Answer any FIVE full questions.***

1 a. Define the pre-envelope. Show the spectral representation of pre-envelopes for low pass signal. **(06 Marks)**

b. Define Hilbert transform. State and prove its properties. **(06 Marks)**

c. For the binary data 10011101, sketch the following :
i) RZ unipoler
ii) NRZ polar
iii) NRZ Bipolar
iv) Manchester format. **(04 Marks)**

2 a. Derive the expression for power spectral density of polar signaling. **(08 Marks)**

b. Derive the expression for complex low pass representation of band pass system. **(08 Marks)**

3 a. Explain the geometric representation of the signal for N = 2 and M = 3 and explain the various parameters. **(06 Marks)**

b. S.T. correlator outputs are statically independent. **(04 Marks)**

c. What do you mean by match filter receiver? Derive the expression for the impulse response of matched filter receiver. **(06 Marks)**

4 a. Using Gram-Schmitt orthoganalization procedure and find the orthnormal basis function for the signal shown below.

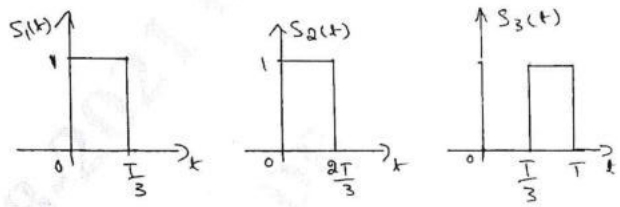

Fig.Q4(a) **(08 Marks)**

b. With neat block diagram explain detector and maximum likelihood decoder of a correlation receiver. **(08 Marks)**

5 a. Explain the generation and detection of BFSK. **(06 Marks)**

b. With the signal space representation of BPSK derive the expression for probability of error. **(06 Marks)**

c. For the input binary sequence 11001001, draw the in phase and quadrature phase components of the QPSK signal. **(04 Marks)**

6 a. With a neat block diagram, explain the generation and coherent detection of QPSK signal. **(06 Marks)**

b. Explain the DPSK transmitter and receiver with neat block diagram. **(06 Marks)**

c. Explain the binary FSK using non coherent detection. **(04 Marks)**

7 a. With a neat diagram of digital PAM system obtain the expression for ISI. **(10 Marks)**
b. State and prove Nquist criterion for zero ISI. **(06 Marks)**

8 a. Explain the design by band limited signals with controlled ISI. **(10 Marks)**
b. With neat diagram and relevant expressions explain the concept of adaptive equalization. **(06 Marks)**

9 a. Explain the model of a spread spectrum digital communication system. **(08 Marks)**
b. A slow frequency Happed/MFSK system has the following parameters
i) The number of bits/MFSK symbol = 4
ii) The number of MFSK symbol per hop = 5
iii)Calculate the processing gain of the system in decibels. **(02 Marks)**
c. List and briefly explain any 3 application of direct sequence spread spectrum. **(06 Marks)**

10 a. With a neat block diagram explain frequency spread spectrum technique. Also explain the terms chiprate, jamming margin and processing gain. **(08 Marks)**
b. Explain the effect of dispreading on a narrow band interference in direct sequence spread spectrum systems.
A DSSS signal in designed to have the power ratio P_R/P_N at the intended receiver is 10^{-2}. If the desired $E_b/N_0 = 10$ for acceptable performance. Determine the minimum value of processing gain. **(08 Marks)**

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CBCS SCHEME

USN | | | | | | | | | | |

15EC63

Sixth Semester B.E. Degree Examination, July/August 2021
VLSI Design

Time: 3 hrs. Max. Marks:80

Note: ***Answer any FIVE full questions.***

1 a. Explain the nMOS enhancement mode transistor operation with a neat diagram. **(08 Marks)**

b. Explain the fabrication steps of CMOS P-well process with neat diagram and write the mask sequence. **(08 Marks)**

2 a. Obtain the DC transfer characteristics of a CMOS inverter and mark all the region showing the status of P-MOS and nMOS. **(08 Marks)**

b. What are the advantages of BICMOS process over CMOS technology? **(04 Marks)**

c. Explain the following :
i) Channel length modulation
ii) Noise margin. **(04 Marks)**

3 a. Explain λ based design rules with a neat diagram. **(08 Marks)**

b. Draw the schematic, stick diagram and lay out for a CMOS inverter. **(08 Marks)**

4 a. Derive the expression for sheet resistance. **(04 Marks)**

b. Derive an expression for the estimation of CMOS inverter delay. **(08 Marks)**

c. Write a short note on super Buffers. **(04 Marks)**

5 a. Find the scaling factors for :
i) Saturation current
ii) Current density
iii) Power dissipation/unit area
iv) Maximum operating frequency. **(08 Marks)**

b. With a neat diagram, explain 4 × 4 barrel shifter. **(08 Marks)**

6 a. Design a 4 bit ALU to implement addition subtraction, EX – OR, EX-NOR, OR and AND operation. **(08 Marks)**

b. Describe Manchester carry-chain. **(08 Marks)**

7 a. Discuss the architectural issues related to subsystem. **(08 Marks)**

b. Explain switch logic implementation of a 4 × 4 Four way multiplexer. **(08 Marks)**

8 a. Explain FPGA architecture. **(08 Marks)**

b. Explain parity generator with basic block diagram and stick diagram. **(08 Marks)**

9 a. Explain Pseudo-static RAM cell (NMOS) with schematic and stick diagram. **(08 Marks)**

b. Write a note on testability and testing. **(08 Marks)**

10 a. Explain three-transistor dynamic RAM cell with schematic and stick diagram. **(08 Marks)**

b. List the system timing consideration. **(04 Marks)**

c. Write short note on Built in Self Test [BIST]. **(04 Marks)**

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CBCS SCHEME

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15EC64

Sixth Semester B.E. Degree Examination, July/August 2021
Computer Communication Networks

Time: 3 hrs. Max. Marks:80

Note: ***Answer any FIVE full questions.***

1 a. Explain different types of switched networks used in computer networks with relevant diagrams. **(04 Marks)**

b. Explain layers of TCP/IP protocol suite with relevant diagram. **(10 Marks)**

c. Assume a system uses five protocol layers. If the application program creates a message of 100 bytes and each layer adds a header of 10 bytes to the data unit, what is the efficiency of the system? **(02 Marks)**

2 a. Explain with necessary diagram show ARP protocol finds link layer address of next node in a network. **(07 Marks)**

b. Explain the need for sequence number and acknowledgment numbers in stop-and-wait protocol with FSM and flow diagram. **(07 Marks)**

c. Unstuff the following frame where payload in which 'E' is Escape byte, 'F' is the flag byte, and 'D' is a data byte other than an escape or a flag character.

E	E	D	E	F	D	D	E	F	E	E	D	D	D

(02 Marks)

3 a. Explain behavior of three persistence methods with timing and flow diagram. **(06 Marks)**

b. Show with frame exchange time diagram, how CSMA/CA solves hidden station problem. **(06 Marks)**

c. Assume that there are three active stations in a slotted ALOHA network : A, B and C. Each station generates a frame in a time slot with the corresponding probabilities $P_A = 0.2$, $P_B = 0.3$, $P_C = 0.4$ respectively.

i) What is the throughput of each station?

ii) What is the throughput of the network? **(04 Marks)**

4 a. Explain IEEE 802.3 frame format with neat diagram. **(06 Marks)**

b. Explain with suitable diagram, 10 base 2 and 10 base 5 physical layer implementations in 10 Mbps Ethernet. **(06 Marks)**

c. A network with one primary and four secondary station uses polling. The size of a data frame is 1000bytes. The size of the poll, ACK and NAK frames are 32 bytes each. Each station has 5 frames to send. How many total bytes are exchanged if there is no limitation on the number of frames a station can send in response to a poll? **(04 Marks)**

5 a. Explain with neat diagram IEEE802.11 addressing mechanism. **(06 Marks)**

b. Show with examples how redundant switches create loops in transparent switches. **(06 Marks)**

c. In an 802.11 communication, the size of the payload is 1200 bytes. The station decides to fragment the frame into three fragments, each of 400 payload bytes. Answer the following questions :

i) What would be the size of the data frame with fragmentation?

ii) What is the size of each frame after fragmentation?

iii) How many total bytes are sent after fragmentation?

iv) How many extra bytes are sent because of fragmentation? **(04 Marks)**

6 a. Explain with a neat diagram, three types of baseband layer formats. **(06 Marks)**

b. Explain DHCP message format with neat diagram. **(04 Marks)**

c. An organization is granted the block 16.0.0.0/8. The administrator wants to create 500 fixed length subnets

i) Find the subnet mask

ii) Find the number of addresses in each subnet

iii) Find the first and last address in subnet 1

iv) Find the first and last address in subnet 500. **(06 Marks)**

7 a. Show general formats of ICMP messages and explain query messages. **(08 Marks)**

b. With neat diagram, mention three phases in remote host and mobile host communication. **(04 Marks)**

c. In a IPv4 datagram, the M bit is 0, the value of HLEN is 5, the value of total length is 200, and the offset value is 200, what is the number of the first byte and number of the last byte? Is this the last fragment? **(04 Marks)**

8 a. Explain methods to overcome count-to-infinity problem considering two-node instability example with neat diagram. **(06 Marks)**

b. Using Dijkstra's algorithm find the shortest path tree and the forwarding table for node 'A' in Fig.Q8(b).

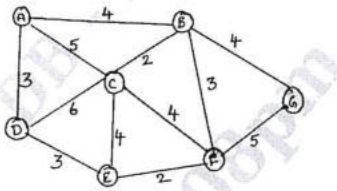

Fig.Q8(b) **(10 Marks)**

9 a. Why window size in selective repeat protocol should be equal to $2^{(m-1)}$, prove your answer with flow diagram. **(06 Marks)**

b. Design Go-Back-N sliding–window protocol for a network in which the bandwidth is 100Mbps and the average distance between the sender and receiver is 10,000km. Assume the average packet size is 100,000 bits and the propagation speed in the media is 2×10^8m/s. Find the maximum size of the send and receive windows, the number of bits in the sequence number field (m), and an appropriate time-out value for the timer. **(06 Marks)**

c. Show TCP segment format with neat diagram. **(04 Marks)**

10 a. Explain steps involved in three – way handshaking during connection establishment in TCP protocol. **(08 Marks)**

b. A client use UDP to send data to a server. The data length is 16 bytes. Calculate the efficiency of this transmission at the UDP level. **(02 Marks)**

c. The following is part of a TCP header dump (contents) in hexadecimal format :

E2930017	00000001	00000000	500207FF

i) What is the source port number?

ii) What is the destination port number

iii) What is sequence number?

iv) What is the acknowledgment number?

v) What is the length of the header?

vi) What is the type of the segment?

vii) What is the window size? **(06 Marks)**

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15EC655

Sixth Semester B.E. Degree Examination, July/August 2021
Microelectronics

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions.

1 a. Derive an expression of drain current in NMOS transistor for triode and saturation regions, with necessary diagrams. **(08 Marks)**

b. Design the circuit shown in Fig.Q1(b) to obtain a current I_D of 80 μA. Find the value required for R and find the dc voltage V_D. Let the NMOS transistor have V_t = 0.6 V, $\mu_n C_{ox}$ = 200 μA/V^2, L = 0.8 μm and w = 4 μm. Neglect the channel-length modulation effect (i.e. assume $\lambda = 0$).

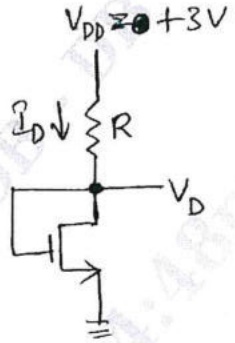

Fig.Q1(b) **(04 Marks)**

c. Explain the effect of substrate bias on threshold voltage of MOS transistors. **(04 Marks)**

2 a. With a neat diagram, explain the operation of enhancement-type NMOS transistor in detail. **(08 Marks)**

b. An NMOS transistor is fabricated in a 0.4 μm process having $\mu_n C_{ox}$ = 200 μA/V^2 and V'_A = 50 V/μm of channel length. If L = 0.8 μm and W = 16 μm, find V_A and λ. Find the value of I_D that results when the device is operated with an overdrive voltage V_{OV} = 0.5 V and V_{DS} = 1V. Also find the value of r_0 at this operating point. If V_{DS} is increased by 2V, what is the corresponding change in I_D? **(08 Marks)**

3 a. With a neat diagram, explain the operation of the common-source amplifier. Also derive the expressions for input and output resistance and voltage gain. **(10 Marks)**

b. Explain briefly the MOSFET internal capacitances. **(06 Marks)**

4 a. Explain the biasing of MOSFET using constant current source. **(06 Marks)**

b. Explain the small signal model of MOSFET and how the T-equivalent circuit model can be obtained. **(06 Marks)**

c. A MOSFET is to operate at I_D = 0.1 mA and is to have g_m = 1 mA/V. If K'_n = 50 μA/V^2, find the required (W/L) ratio and the overdrive voltage. **(04 Marks)**

5 a. Compare the following characteristics of MOSFET and BJT:
(i) Transconductance g_m
(ii) Intrinsic gain A_o **(04 Marks)**

b. Given $V_{DD} = 3V$ and using $I_{Ref} = 100\ \mu A$, it is required to design the circuit of Fig.Q5(b) to obtain an output current whose nominal value is 100 μA. Find R if Q_1 and Q_2 are matched and have channel lengths of 1 μm, channel widths of 10 μm, $V_t = 0.7$ V, and $K_n' = 200\ \mu A/V^2$. What is the lowest possible value of V_0? Assuming that for this process technology the early voltage $V_A' = 20$ V/μm, find the output resistance of the current source. Also, find the change in output current resulting from a +1V change in V_0.

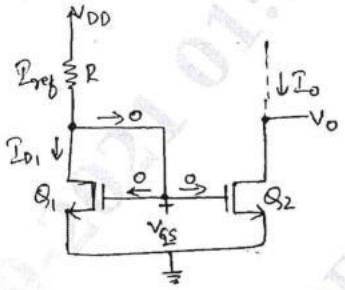

Fig.Q5(b) **(06 Marks)**

c. Derive the expression for determining the 3-dB frequency (ω_H) of an amplifier. **(06 Marks)**

6 a. Explain briefly the operation of MOS current steering circuit. **(06 Marks)**

b. For the circuit shown in Fig.Q6(b), find the midband voltage gain $A_m = V_0/V_{sig}$ and the upper 3-dB frequency f_H. Where $R_{sig} = 100\ K\Omega$, $R_{in} = 420\ K\Omega$, $C_{gs} = C_{gd} = 1$ PF, $g_m = 4$ mA/V and $R_L' = 3.33\ K\Omega$.

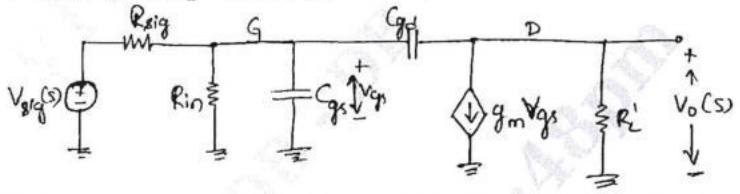

Fig.Q6(b) **(06 Marks)**

c. The high frequency response of an amplifier is characterized by the transfer function.

$$F_H(s) = \frac{1 - \frac{s}{10^5}}{\left(1 + \frac{s}{10^4}\right)\left(1 + \frac{s}{4} * 10^4\right)}$$

Determine the 3-dB frequency approximately and exactly. **(04 Marks)**

7 a. Explain the high frequency response of the CS amplifier and analyze using Miller's theorem. **(08 Marks)**

b. Consider a common-gate amplifier specified as follows:
$W/L = 7.2\ \mu m/0.36\ \mu m$, $K_n' = 387\ \mu A/V^2$, $r_0 = 18\ K\Omega$, $I_D = 100\ \mu A$, $g_m = 1.25$ mA/V, $x = 0.2$, $R_S = 10\ K\Omega$, $R_L = 100\ K\Omega$, $C_{gs} = 20$f F, $C_{gd} = 5$f F and $C_L = 0$. Find A_{V_0}, R_{in}, R_{out}, G_v, G_{is}, G_i and f_H. **(08 Marks)**

8 a. Explain the operation of MOS cascode amplifier. **(08 Marks)**

b. Explain the effect of source resistance on transconductance and voltage gain of a CS amplifier. **(08 Marks)**

9 a. Explain the operation of MOS differential pair with a common mode input voltage. **(08 Marks)**

b. Explain the effect of g_m mismatch on CMRR of a MOS differential amplifier. **(08 Marks)**

10 a. With a neat diagram, explain the operation of a two-stage CMOS op-amp. **(08 Marks)**

b. Obtain the expression for differential gain of the active-loaded MOS pair. **(08 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, July/August 2021
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions.***

1 a. Explain logic and static load levels constraints imposed in Real World circuits. **(08 Marks)**
b. Develop a verilog model for a 7-segment decoder, that includes an additional input "BLANK" that overrides the BCD input and causes all segments not to be lit. **(08 Marks)**

2 a. What is state transition diagram? Explain with Moore and Mealy style output values. **(08 Marks)**
b. Develop a verilog model of a debouncer for a push button switch that uses a debounce interval of 10ms. Assume the system clock frequency is 50MHz. **(08 Marks)**

3 a. Explain Asynchronous static RAM timing methodology. **(08 Marks)**
b. Develop a verilog model of a dual port, 4K × 16bit flow – through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(08 Marks)**

4 a. Explain different types of ROMS. **(08 Marks)**
b. Design a 64K× 8bit composite memory using 4-16K × 8 bit components. **(08 Marks)**

5 a. Explain internal circuit of a PAL16L8 component. **(08 Marks)**
b. Design and explain the circuit for a slice within a logic block of Xilinx Spartan – II FPGA. **(08 Marks)**

6 a. What design techniques can be used to Mitigate Transmission – line effects, such as over shoot, undershoot and ringing? **(04 Marks)**
b. Briefly explain internal organization of CPLD. **(04 Marks)**
c. Design a priority encoder that has 16 inputs, I[0:15]; a 4-bit encoded output, Z[3:0]; and a valid output that is '1' when any input is '1'. Input I[0] has the highest priority and I[15] the lowest priority. The design is to be implemented in a GAL22V10 component. **(08 Marks)**

7 a. Explain four different serial interface standards. **(08 Marks)**
b. Explain how we could decode a BCD value to drive the seven segments of a digit. **(08 Marks)**

8 a. Explain the following I/O synchronization techniques i) Polling ii) Timers. **(06 Marks)**
b. With a neat sketch describe R-string DAC. **(06 Marks)**
c. Explain distributed Multiplexer bus standard. **(04 Marks)**

9 a. Explain the purpose of floor planning, placement and routing of physical Design. **(06 Marks)**
b. Explain JTAG boundary scan cell for an input or output pin. **(06 Marks)**
c. Explain Hardware Abstraction Layer (HAL) Instruction Set Simulator (ISS) for Embedded System Software in brief. **(04 Marks)**

10 a. Explain 4-bit CFSR for generating Pseudo – random test vectors of BIST concept. **(08 Marks)**
b. What changes must be made to a circuit to create a scan chain? Explain in detail. **(08 Marks)**

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